REMARKS

Claims 1-2, 4-11 and 13-21 remain pending herein. Claims 3, 12 and 22-53 have been canceled.

Claims 1, 2, 12-17, 19 and 20 were rejected under 35 U.S.C. Section 103(a) over Goldstein et al. This rejection is moot in view of the incorporation of the subject matter of claim 3 into claim 1.

Claims 3-11, 18 and 21 were rejected under 35 U.S.C. Section 103(a) over Goldstein et al. in view of Bosch. This rejection is respectfully traversed for the following reasons.

The claimed invention is drawn to a semiconductor processing component comprising SiC, having an outer surface portion that consists essentially of CVD-SiC and a surface impurity level not greater than 5 times a bulk impurity level. As discussed in the present specification, the claimed semiconductor processing component has been developed to provide improved processability of semiconductor components, notably by reducing component impurity levels along a critical portion of the component, the outer surface portion of the component. The semiconductor processing component notably includes an outer surface portion that consists essentially of CVD-SiC, which may be in the form of a deposited CVD-SiC layer overlying a substrate such as a Si/SiC substrate (claims 4-9). Alternatively, the component may be a free-standing CVD-SiC component, substantially the entirety of which is formed by CVD (claim 10). In either case, the semiconductor processing component is formed to have a notably reduced surface impurity level. As described in the present specification, Applicants have discovered that conventional CVD processing results in a spike in impurity levels along the outer surface of the CVD-SiC layer. According to embodiments of the present invention, through additional processing, such as by removal of a target portion of the CVD-SiC forming the outer surface portion, outer surface impurity levels are noticeably reduced. For example, impurity levels are reduced to be not greater than 5 times a bulk impurity level, or not greater than 2 times a bulk impurity level (claim 13), or even not greater than the bulk impurity level (claim 14).

The primary reference Goldstein et al. discloses a Si/SiC component that is formed by conventional silicon impregnation processing, in which a porous silicon carbide body is impregnated with molten silicon to form a composite Si/SiC body. Goldstein et al. teach that the SiC grains may be purified by maintaining the impregnated body at a high temperature to cause diffusion of impurities from the silicon carbide grains into the silicon fill followed by removal of the now contaminated silicon fill (e.g., by etching), and subsequent deposition of a clean silicon fill (see col. 3, lines 5-20 of Goldstein et al.). Goldstein et al. fail to disclose (or even remotely suggest) a silicon carbide semiconductor processing component having an outer surface portion consisting of essentially a CVD-SiC. Accordingly, the PTO has looked to Bosch.

Bosch teaches that semiconductor processing equipment may be formed by CVD of SiC. The PTO argues that it would be obvious to utilize such processing in the context of Goldstein et al. Foremost, Applicants do not dispute the wide use of CVD-SiC in the context of semiconductor processing components. However, use CVD-SiC in light of Goldstein et al. fails to even remotely suggest all features of the claimed invention. Goldstein et al. teach a process of impurity reduction along an outer surface of a Si/SiC composite through a silicon fill subtractive process, not impurity reduction along an outer surface portion consisting of essentially a CVD-SiC. There is no teaching or even remote suggestion of impurity reduction of a CVD-SiC outer portion, let alone any enabling disclosure as to how one of ordinary skill in the art could even remotely achieve impurity reduction in the context of CVD-SiC. Goldstein et al. rely upon impurity migration into a silicon fill. However, CVD-SiC of Bosch has no silicon fill (and is incompatible with a silicon fill), and accordingly, use of CVD-SiC precludes the purification mechanism of Goldstein et al. At best, the references suggest that SiC may be chemical vapor deposited to overlie the composite Si/SiC component of Goldstein et al. However, such deposition of a CVD-SiC layer does not even remotely meet the features of the claimed invention, requiring impurity reduction of a CVD-SiC outer surface portion.

For at least of the foregoing reasons in view of the amendments to the present claims, Applicants respectfully submit that the presently claimed invention would not have been obvious over Goldstein et al in view of Bosch. Accordingly, withdrawal of the Section 103(a) rejection is respectfully requested.

Applicants respectfully submit that the present application is now in condition for allowance. Accordingly, the Examiner is requested to issue a Notice of Allowance for all pending claims.

Should the Examiner deem that any further action by the Applicants would be desirable for placing this application in even better condition for issue, the Examiner is requested to telephone the Applicants' undersigned representative at the number below.

The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account Number 50-2469.

Respectfully submitted,

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Date

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